Clint L. Schow – Research Interests

My research interests and directions have evolved and expanded throughout my career, but a central theme has always been the close integration of high-speed electronics and photonics, encompassing circuit and optoelectronic device design and co-optimization and the development of novel packaging to enable higher levels of integration. Moving forward, this focus on integration will become even more critical as the tighter coupling of photonics and electronics is the only path to sustain the aggressive performance trajectory of computing and networking that Moore's law has enabled for the past decades.

Background - Optoelectronic/Electronic Integration

My Ph.D. work to demonstrate monolithically integrated Si optical receivers stressed integration, demanding that I gain both device engineering and high-speed analog circuit design skills. My first job was in product development for IBM's optical transceiver division (Rochester, MN) with full and direct responsibility for all the optical receivers across multiple product lines that totaled more than $100M in annual revenue. In my two-year stint I learned how to practically apply the knowledge I had gained in school, and most importantly what it takes to develop and ship a successful product – limited not just to R&D, but ensuring reliability, driving standards development, listening to and supporting customers, and developing supplier relationships. I then joined Agility Communications (Santa Barbara, CA) where my focus shifted to photonic integration as I played a primary role in the high-speed chip and package design for 2.5 Gb/s electro-absorption modulators (EAMs), 10 Gb/s Mach-Zehnder, and 40 Gb/s traveling-wave modulator designs.

High-Speed Circuit Design Enabling Highly-Integrated Transceivers

In my early years at IBM Research (Yorktown Heights, NY), in close collaboration with a small, core group of colleagues, I designed generations of highly-integrated multi-mode VCSEL-based parallel optical transceivers. Although it was not the skill for which I was hired, it was immediately clear to me when I joined IBM that circuit design was critically lacking in our group. Driven by a desire to build the fastest and most integrated transceivers in the world, I worked to expand my circuit design skills from schematics and simulation to physical layout. I spent the majority of my time designing chips, and when they returned from fabrication, characterizing optical assemblies incorporating them. The transceivers I designed set records for aggregate bandwidth (reaching 1 Tb/s) per-channel speed (up to 40 Gb/s), link power efficiency (as low as 7.3 pJ/bit wall-plug), and bandwidth density (as high as 32 Gb/s/mm^2).[1] I also continually strived to improve the performance of VCSEL links, designing circuits in multiple generations of CMOS and in SiGe bipolar technologies. I built the first CMOS-driven optical links to operate above 25 Gb/s, employed new applications of transmitter equalization to simultaneously improve all aspects of link performance (speed, jitter, margin, and power efficiency), and demonstrated the first complete VCSEL links (laser driver IC + VCSEL to photodiode + receiver IC) operating above 30 Gb/s, eventually reaching a record 71 Gb/s.[2]

Beyond multi-mode VCSEL interconnects, I was heavily involved in the seminal years of IBM Research's Si photonic technology development. My responsibility and contribution was designing 90-nm CMOS circuits: high-speed drivers for ring resonator and Mach-Zehnder modulators, receiver circuits tuned for waveguide Ge detectors, and digital drivers for multi-port optical switches.[3]

[1] F. E. Doany, B. G. Lee, D. M. Kuchta, A. V. Rylyakov, C. Baks, C. Jahnes F. Libsch, C. L. Schow," Terabit/Sec VCSEL-based 48-channel optical module based on holey CMOS transceiver IC," IEEE J. of Lightw. Technol., vol. 31, no. 4, pp.672-680, Feb. 2013. (86 citations)

[2] D. Kuchta, A. Rylyakov, F. Doany, C. L. Schow, J. Proesel, C. Baks, P. Westbergh, J. Gustavsson, A. Larsson, "A 71 Gb/s NRZ Modulated 850 nm VCSEL-based Optical Link," IEEE Photon. Technol. Lett., vol. 27, no. 6, pp 577-580, Mar. 2015. (309 citations)

[3] B. G. Lee, A. V. Rylyakov, W. M. J. Green, S. Assefa, C. W. Baks, R. Rimolo-Donadio, D. M. Kuchta, M. H. Khater, T. Barwicz, C. Reinholm, E. Kiewra, S. M. Shank, C. L. Schow, Y. A. Vlasov, "Monolithic Silicon Integration of Scaled Photonic Switch Fabrics, CMOS Logic, and Device Driver Circuits," *IEEE J. of Lightw. Technol.*, vol. 32, no. 4, pp.743-751, Feb. 2014. (149 citations)

Holistic Design of Electronic/Photonic I/O

The trend for optics displacing copper interconnects at ever-shorter distances will continue, photonic links will be deployed in ever greater volumes, and their importance in computer and data center networks will only increase. My experience in building transceivers has led me to the strong conclusion that to enable the interconnect bandwidths (TB/s) and efficiencies (sub-pJ/bit) required by future systems, a holistic approach must be undertaken in developing the critical underlying electronic and photonic technologies. The problem of transporting high-speed data can no longer be segmented and compartmentalized into 50-ohm interfaces separating digital chips from analog drive electronics and photonics.[4]

New Functionalities for Application-Level Impact

Developing highly-optimized integrated electronic/photonic I/O is critical to enable future high performance computers and data centers. However, I've always been interested in finding ways to move beyond demonstrating optical interconnect technologies that can be categorized as just better "wires," compared to copper interconnects, to developing photonics with unique functionality that can be leveraged to yield compelling system-level performance advantages. Research on photonics for data centers and computing should be targeted at enhancing function and flexibility in the optical network. In my last years at IBM, I was PI for a multi-million dollar DARPA-funded program (TOPS) focused on developing a low-latency and scalable photonic switch fabric to yield orders of magnitude improvement on data analytics workloads.[5] The switch platform embodied a focus on the integration and co-design of multiple technologies: III-V semiconductor optical amplifiers (SOAs) to provide integrated gain and overcome losses, Si photonics for efficient switching, WDM and coupling structures, and CMOS drive electronics for configuration and control.[6]

Current Focus

One of my largest current projects, funded by ARPA-E, is a collaboration with Facebook aimed at demonstrating a technology platform to directly integrate power-efficient coherent photonic I/O into chip packages to enable larger radix switches.[7] The coherent links we are developing are based on optical phase locked loops and are optimized based on critical metrics for the datacenter: 1) low power consumption, 2) a factor of up to 20dB improvement in optical link budget 3) low cost, 4) low latency, and 5) future bandwidth scalability through higher-order modulation. Significantly larger optical link budgets are a key advantage with the potential to enable novel network architectures incorporating all-optical routing/switching. This project illustrates what I believe to be an ideal model for research, coupling a bottom-up technology push to develop devices and subsystems offering new enabling functionality with a top-down system architecture and application pull that frames a believable and compelling story.

[4] A. Ramaswamy, J. E. Roth, E. J. Norberg, R. S. Guzzon, J. H. Shin, J. T. Imamura, B. R. Koch, D. K. Sparacin, G. A. Fish, B. G. Lee, R. Rimolo-Donadio, C. W. Baks, A. Rylyakov, J. Proesel, M. Meghelli**, C. L. Schow**, "A WDM 4x28Gbps Integrated Silicon Photonic Transmitter driven by 32nm CMOS driver ICs," *Optical Fiber Communication (OFC) Conference 2015*, Paper Th5B.5, Los Angeles, CA, USA, Mar. 2015. (post deadline paper, 32 citations)

[5] L. Schares, B. G. Lee, F. Checconi, R. Budd, A. Rylyakov, N. Dupuis, F. Petrini, C. L. Schow, P. Fuentes, O. Mattes, C. Minkenberg, "A Throughput-Optimized Optical Network for Data-Intensive Computing," *IEEE Micro*, vol.34, no.5, pp.52-63, Sept.-Oct. 2014. (42 citations)

[6] B. G. Lee, N. Dupuis, P. Pepeljugoski, L. Schares, R. Budd, J. R. Bickford, and C. L. Schow, "Silicon Photonic Switch Fabrics in Computer Communications Systems," *IEEE JLT*, vol. 33, no. 4, pp. 768-777, Feb 2015. (46 citations)

[7] C. L. Schow and K. Schmidtke, "INTREPID: Developing Power Efficient Analog Coherent Interconnects to Transform Data Center Networks," *Optical Fiber Communication (OFC) Conference 2019*, Paper M4D.9, pp. 1-3, San Diego, CA, USA, Mar. 2019.